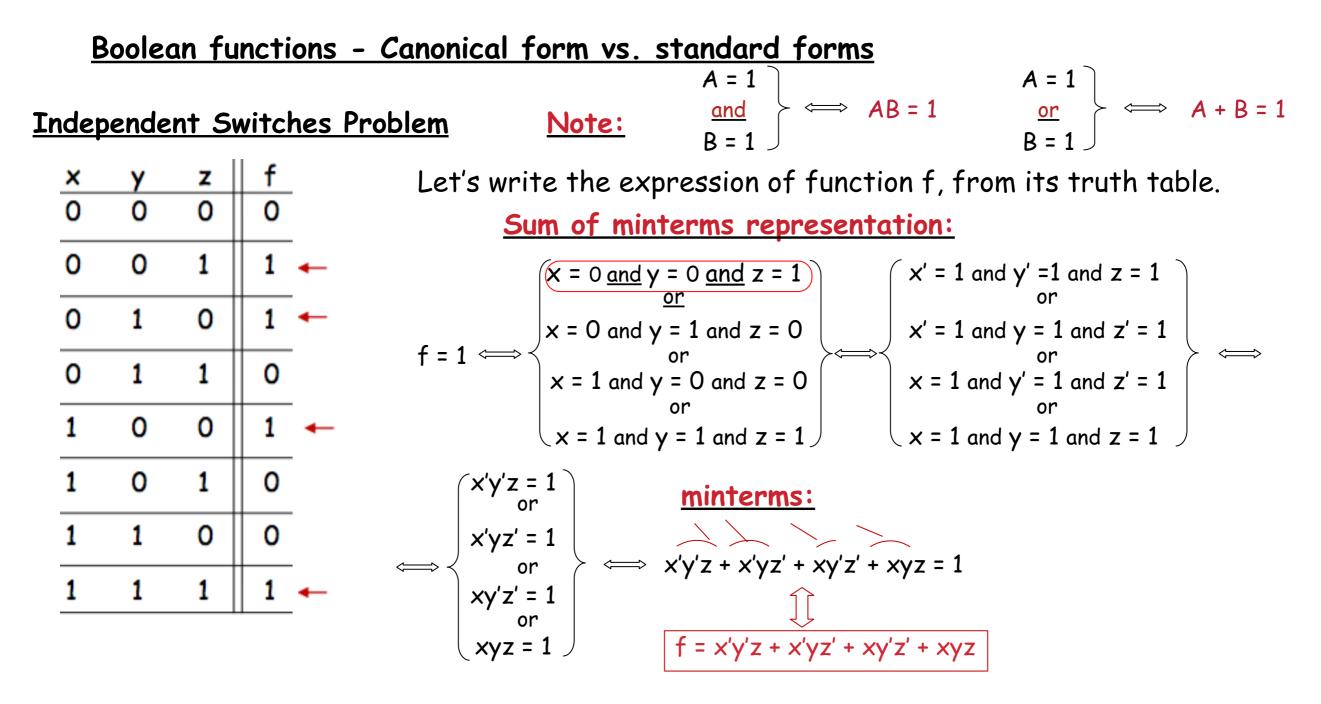
Canonical Standard Forms

CLASS 10



This is called the <u>canonical sum of products</u> form.

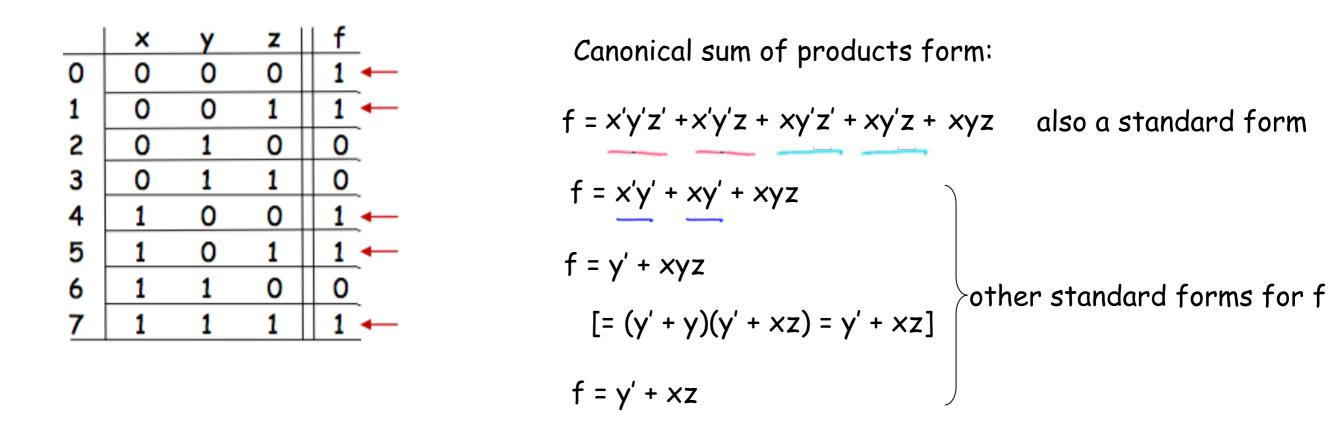
The canonical form is <u>unique</u> for a given function, and it can be used to compare functions/expressions. Most times, the canonical form may be reduced, simplified.

Any sum of products, not necessarily containing only minterms, is called standard.

Similarly, we have a dual form, called the <u>canonical product of sums</u> form; however in this course

we will only deal with the sum of minterms representations, as the other is handled similarly.

Example (Short Cut): Obtain the canonical form directly from the truth table of an arbitrary function



Because the canonical sum of products form is unique we express this function above as:

$$f = \sum (0, 1, 4, 5, 7)$$

Minimization of functions

Time and space trade-offs

Variety of techniques to obtain gate simplification.

<u>However</u>: simplification depends on the <u>metric</u> we use:

- The <u>number of literals</u> it contains
 - = amount of *wiring* needed to implement the function: # inputs: 3-4 usual,
 - > 8,9 very rare.
- The <u>number of gates</u>
 - = strong correlation with <u># components</u> needed for implementation; simplest design to manufacture is the one with fewest gates, not literals.

Number of cascaded levels of gates

= reducing # logic levels would <u>reduce</u> <u>the overall delay</u> in the path input --> output; however an implementation with minimum delay rarely yields an implementation with fewest # literals or gates.

Traditional minimization techniques: reduce delay at expense of adding more gates. Other methods: <u>Trade-off between increased circuit delay and reduced gate count</u>.

Example

F = a'b'c + a'bc + ab'c + abc'

$$F_1$$
 = abc'+a'c+b'c

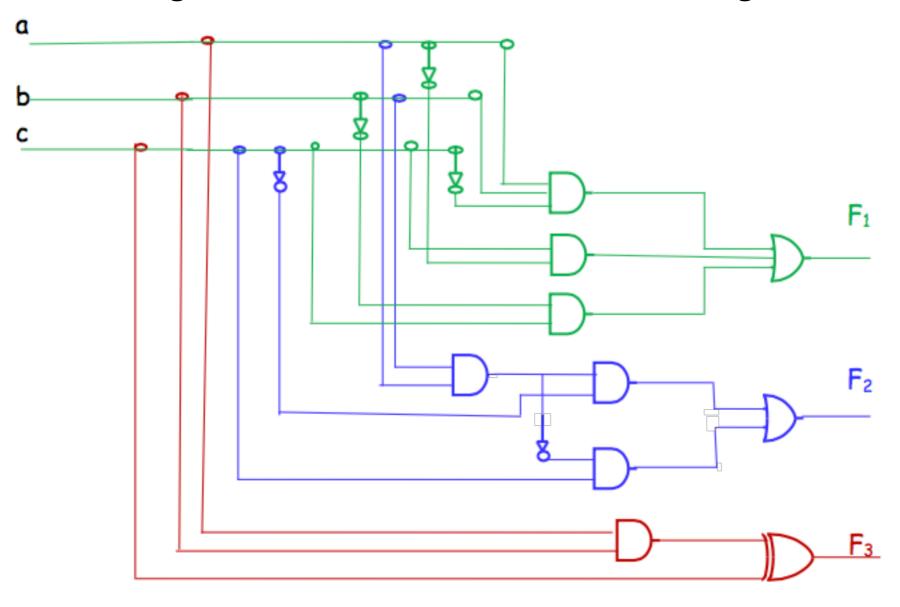
Logical Diagrams (all three functions in one diagram):

- 2-level implementation
- <u>7 literals</u> (<12 as the original)
 - 3-level implementation
 - 4 literals
 - longest path: 4 gates (> 3 in F1)
 --> not as fast as F1.
 - total # gates in $F_2 \leq in F_1$.

 $F_3 = (ab) \bigoplus c$ • XOR = complex gate: implement

- by combining NAND, NOR
- ' lowest gate count, but also

worst signal delay, for XOR slow compared to simple AND, OR.



HW 12 - assigned

- 12-A Given the Boolean functions F_1 and F_2 ,
 - (a) Show that the Boolean function $E = F_1 + F_2$ contains the sum of the minterms of F_1 and F_2 .
 - (b) Show that the Boolean function $G = F_1 F_2$ contains only the minterms that are common to F_1 and F_2 .

12-B Give the truth table of the function:

F = xy + xy' + y'z