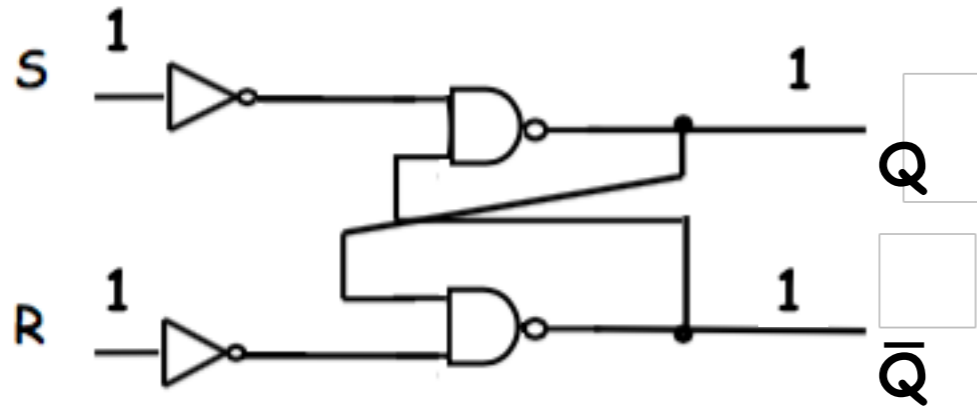


Flip Flops

CLASS 19

HW 19

Evaluate the following flip-flop, by giving its truth table.



Solution

Truth table:

S	R	Q	\bar{Q}
0	0	PS = 0 --> stays 0 PS = 1 --> stays 1	PS
0	1	0	1
1	0	1	0
1	1	1	1

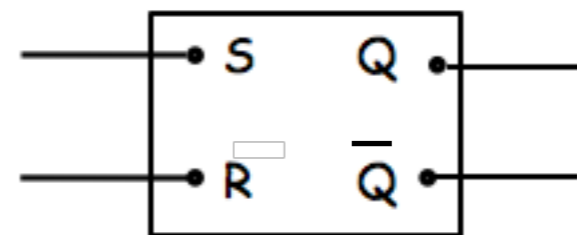
Not allowed !

Exclude the 1-1 input for S-R Flip-Flop, as we cannot have $Q = \bar{Q}$

The truth table then becomes:

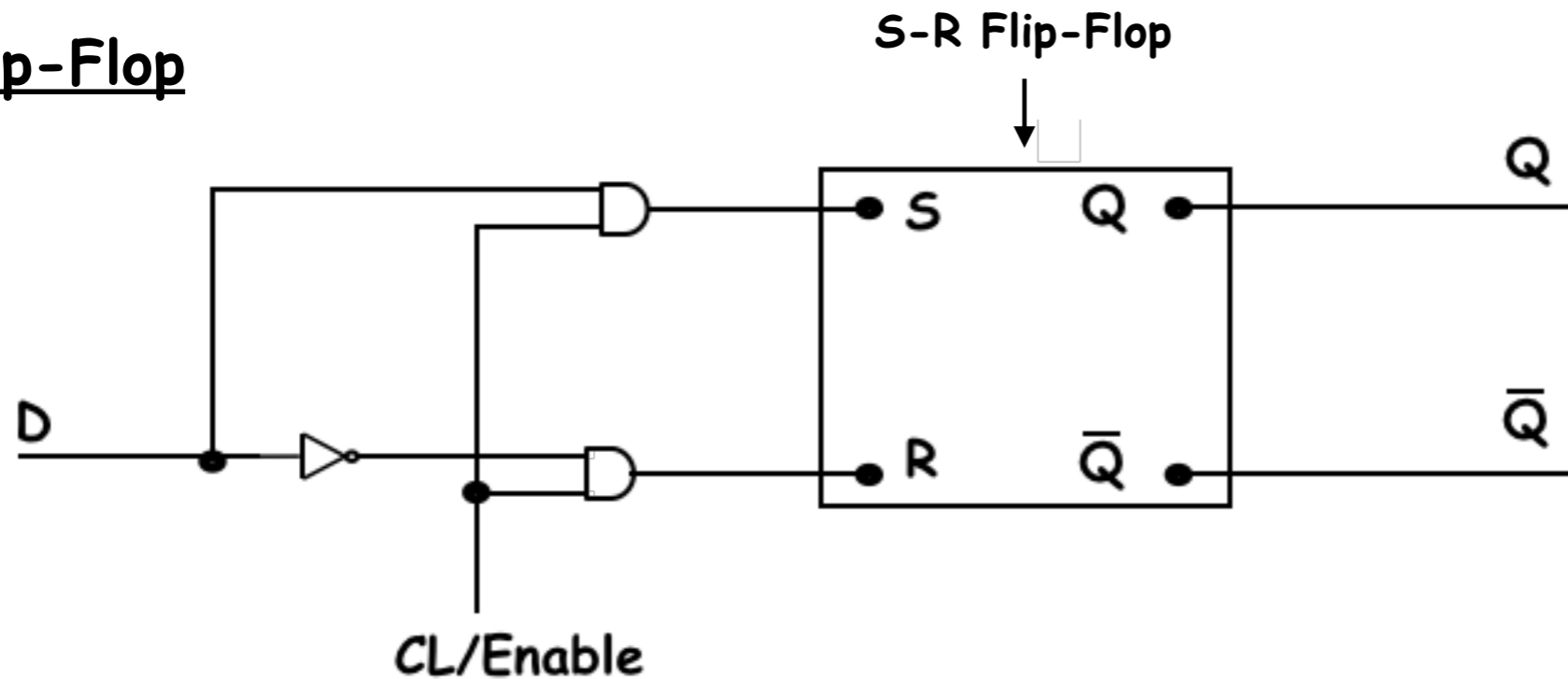
S	R	Q
0	0	PS
0	1	0
1	0	1

From now on the S-R Flip-Flop will be represented by:



Various Flip-Flops

D Flip-Flop

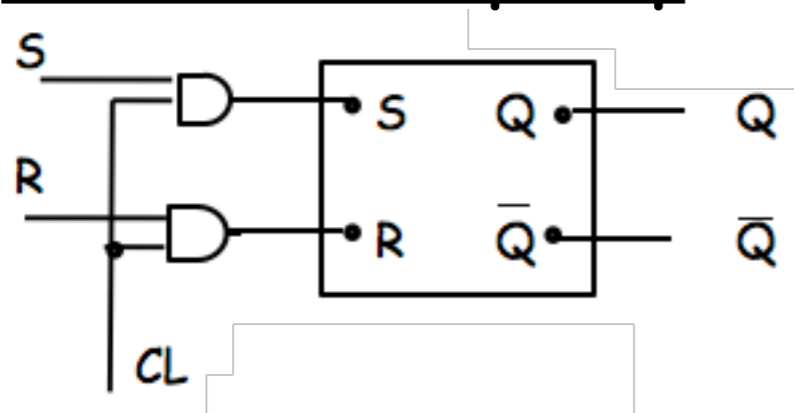


Note: CL/Enable acts as controller. Looking at the CL/Enable values, which inputs are allowed in the S-R flip-flop? $S=D$, and $R=D'$, for $CL=1$, and $S=R=0$, for $CL=0$.

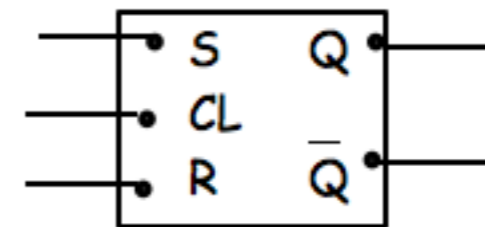
The Problem Input 1-1 is avoided!

CL/Enable	Q
0	PS
1	D

Clocked S-R Flip-Flop



represented by:

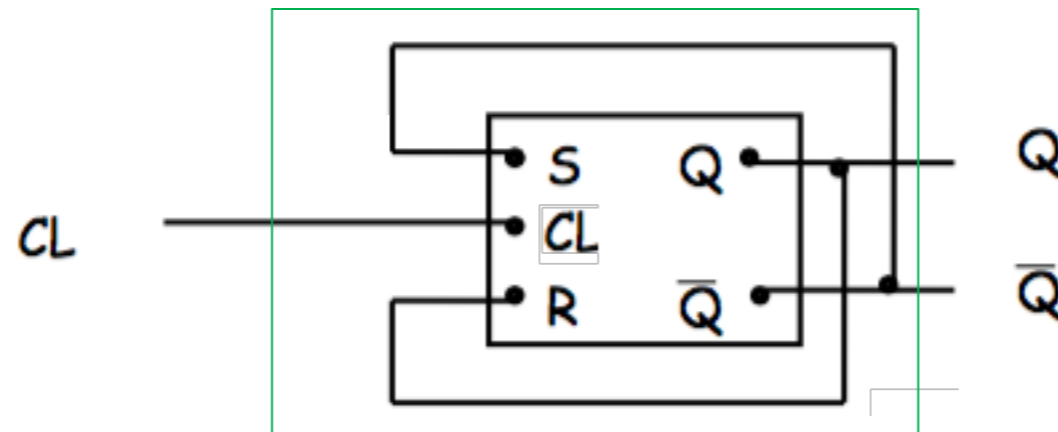


Note: Here input 1-1 is avoided only if $S = \bar{R}$, which is usually the case.

Truth table:

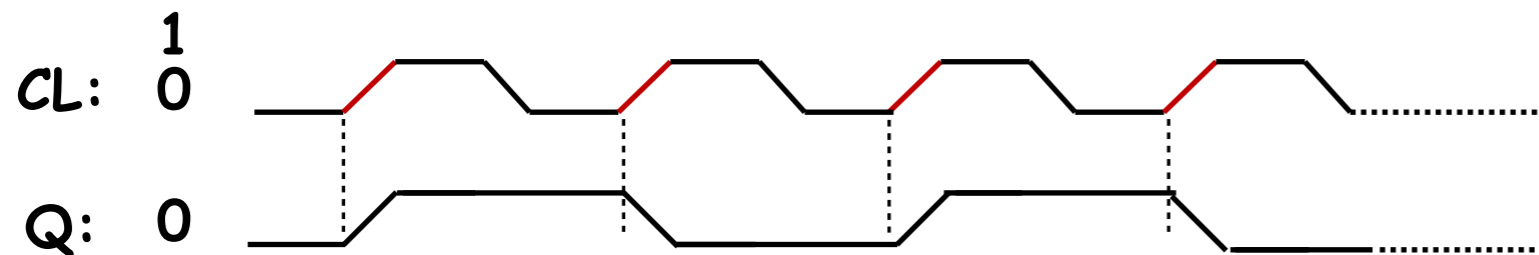
CL	Q
0	PS
1	S

T Flip-Flop



We will represent the input, namely CL , as a diagram, time being one of the coordinates, and $\{0, 1\}$ the other.

We want to give the corresponding diagram for the output Q . We initialize $CL = 0$, and $Q = 0$.



Note:

It is the rising edge (**red**) of the CL that acts as a **1**-input to the CL - S - R flip-flop. Outside the rising edges CL acts as a 0-input to the CL - S - R flip-flop.

That is, **input CL will only enable the S - R flip-flop during the rising edges of CL .**

We exaggerated the duration of the rising edge (**red**) of the CL to show its importance.

Conclusion:

The Q signal oscillates at a speed that is 2 x slower than the CL input.

HW: Start Review for Part II.