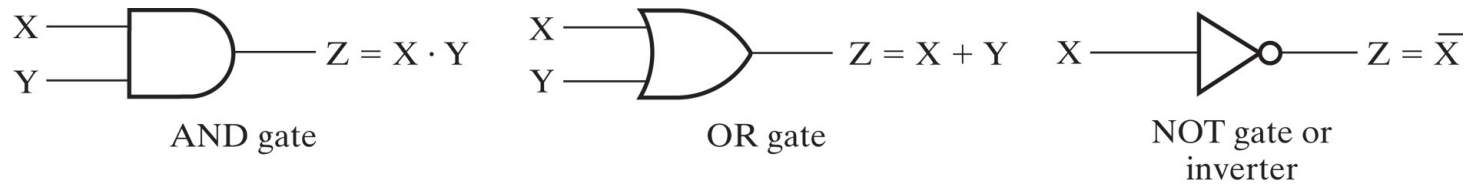
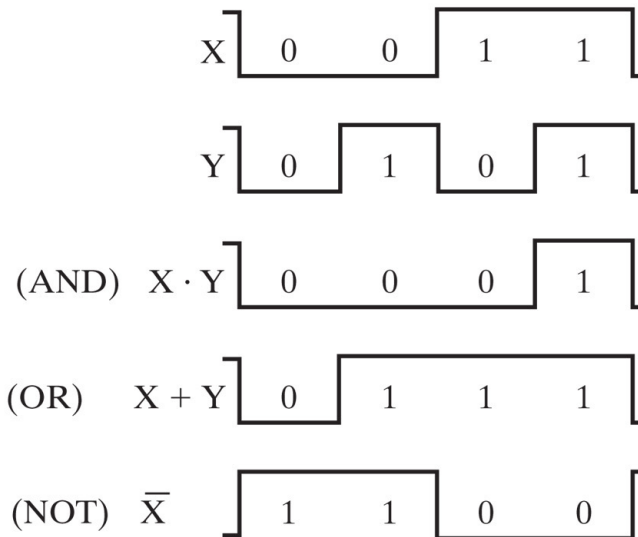


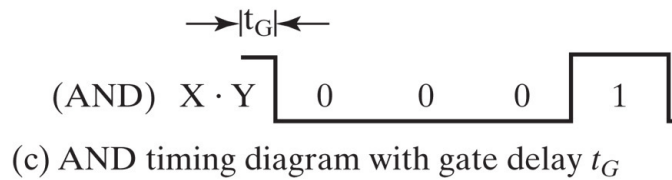
FIGURE 2-1 Digital Logic Gates



(a) Graphic symbols



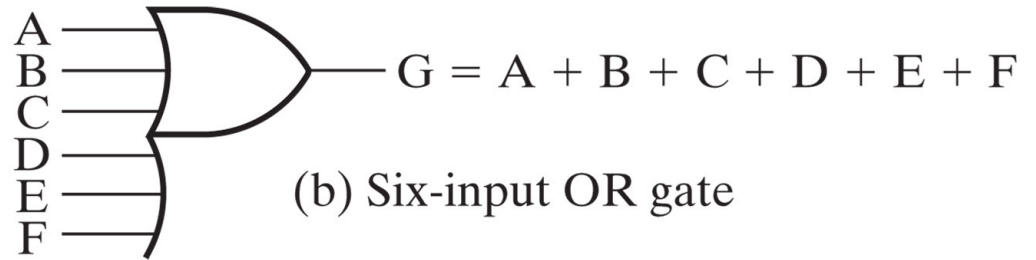
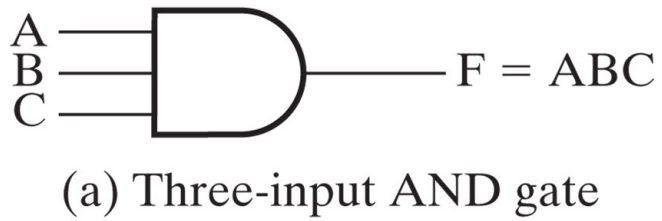
(b) Timing diagram



(c) AND timing diagram with gate delay t_G








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FIGURE 2-2 Gates with More than Two Inputs



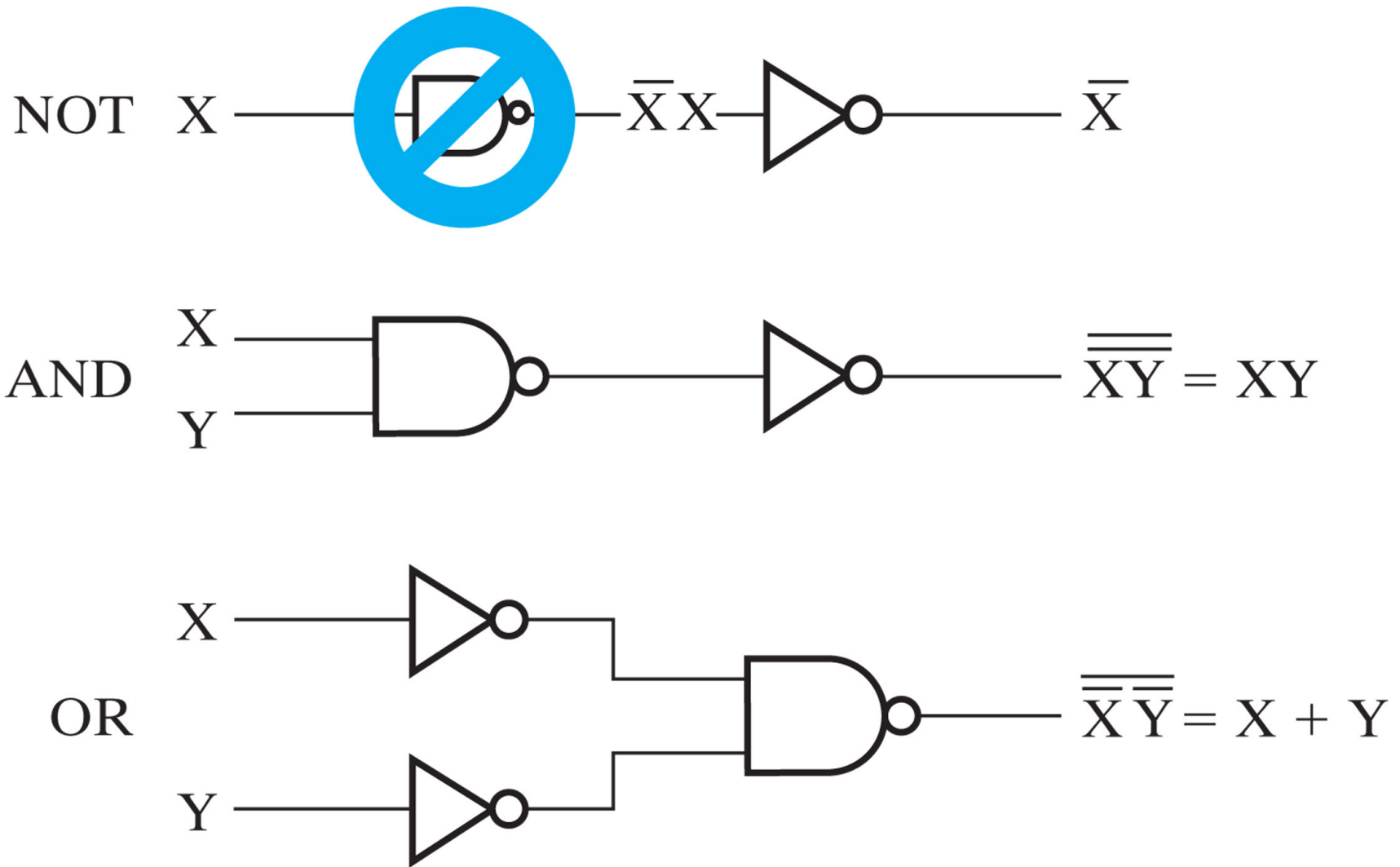
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FIGURE 2-3 Commonly Used Logic Gates

Name	Distinctive-Shape Graphics Symbol	Algebraic Equation	Truth Table															
AND		$F = XY$	<table border="1"> <thead> <tr> <th>X</th> <th>Y</th> <th>F</th> </tr> </thead> <tbody> <tr><td>0</td><td>0</td><td>0</td></tr> <tr><td>0</td><td>1</td><td>0</td></tr> <tr><td>1</td><td>0</td><td>0</td></tr> <tr><td>1</td><td>1</td><td>1</td></tr> </tbody> </table>	X	Y	F	0	0	0	0	1	0	1	0	0	1	1	1
X	Y	F																
0	0	0																
0	1	0																
1	0	0																
1	1	1																
OR		$F = X + Y$	<table border="1"> <thead> <tr> <th>X</th> <th>Y</th> <th>F</th> </tr> </thead> <tbody> <tr><td>0</td><td>0</td><td>0</td></tr> <tr><td>0</td><td>1</td><td>1</td></tr> <tr><td>1</td><td>0</td><td>1</td></tr> <tr><td>1</td><td>1</td><td>1</td></tr> </tbody> </table>	X	Y	F	0	0	0	0	1	1	1	0	1	1	1	1
X	Y	F																
0	0	0																
0	1	1																
1	0	1																
1	1	1																
NOT (inverter)		$F = \overline{X}$	<table border="1"> <thead> <tr> <th>X</th> <th>F</th> </tr> </thead> <tbody> <tr><td>0</td><td>1</td></tr> <tr><td>1</td><td>0</td></tr> </tbody> </table>	X	F	0	1	1	0									
X	F																	
0	1																	
1	0																	
NAND		$F = \overline{X \cdot Y}$	<table border="1"> <thead> <tr> <th>X</th> <th>Y</th> <th>F</th> </tr> </thead> <tbody> <tr><td>0</td><td>0</td><td>1</td></tr> <tr><td>0</td><td>1</td><td>1</td></tr> <tr><td>1</td><td>0</td><td>1</td></tr> <tr><td>1</td><td>1</td><td>0</td></tr> </tbody> </table>	X	Y	F	0	0	1	0	1	1	1	0	1	1	1	0
X	Y	F																
0	0	1																
0	1	1																
1	0	1																
1	1	0																
NOR		$F = \overline{X + Y}$	<table border="1"> <thead> <tr> <th>X</th> <th>Y</th> <th>F</th> </tr> </thead> <tbody> <tr><td>0</td><td>0</td><td>1</td></tr> <tr><td>0</td><td>1</td><td>0</td></tr> <tr><td>1</td><td>0</td><td>0</td></tr> <tr><td>1</td><td>1</td><td>0</td></tr> </tbody> </table>	X	Y	F	0	0	1	0	1	0	1	0	0	1	1	0
X	Y	F																
0	0	1																
0	1	0																
1	0	0																
1	1	0																
Exclusive-OR (XOR)		$F = X\overline{Y} + \overline{X}Y$ $= X \oplus Y$	<table border="1"> <thead> <tr> <th>X</th> <th>Y</th> <th>F</th> </tr> </thead> <tbody> <tr><td>0</td><td>0</td><td>0</td></tr> <tr><td>0</td><td>1</td><td>1</td></tr> <tr><td>1</td><td>0</td><td>1</td></tr> <tr><td>1</td><td>1</td><td>0</td></tr> </tbody> </table>	X	Y	F	0	0	0	0	1	1	1	0	1	1	1	0
X	Y	F																
0	0	0																
0	1	1																
1	0	1																
1	1	0																
Exclusive-NOR (XNOR)		$F = XY + \overline{X}\overline{Y}$ $= X \oplus Y$	<table border="1"> <thead> <tr> <th>X</th> <th>Y</th> <th>F</th> </tr> </thead> <tbody> <tr><td>0</td><td>0</td><td>1</td></tr> <tr><td>0</td><td>1</td><td>0</td></tr> <tr><td>1</td><td>0</td><td>0</td></tr> <tr><td>1</td><td>1</td><td>1</td></tr> </tbody> </table>	X	Y	F	0	0	1	0	1	0	1	0	0	1	1	1
X	Y	F																
0	0	1																
0	1	0																
1	0	0																
1	1	1																

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FIGURE 2-4 Logical Operations with NAND Gates



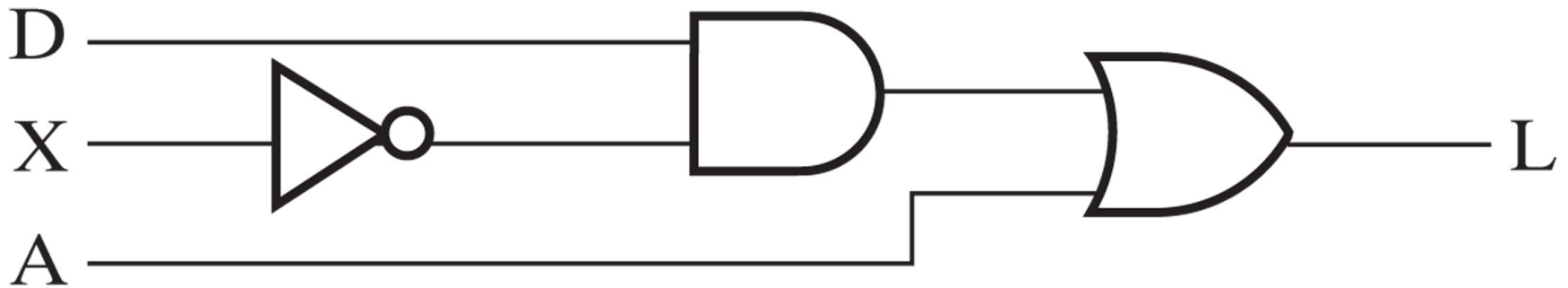
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□ TABLE 2-5

Truth Table for the Function $L = D\bar{X} + A$

D	X	A	L
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	0
1	1	1	1

FIGURE 2-5 Logic Circuit Diagram for $L = DX + A$



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□ TABLE 2-6
Basic Identities of Boolean Algebra

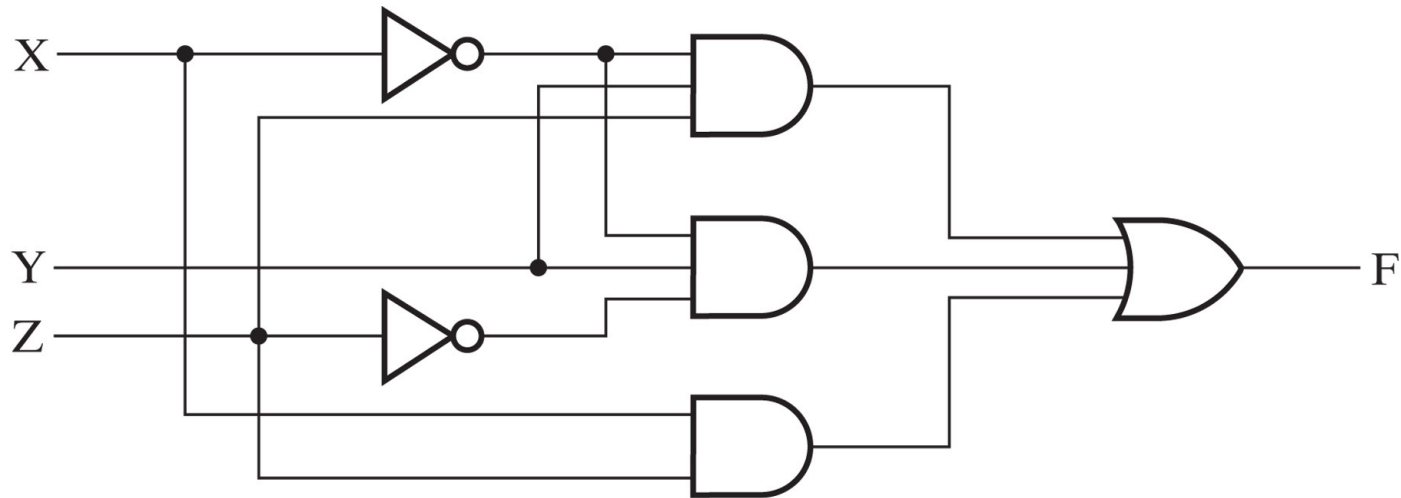
1.	$X + 0 = X$	2.	$X \cdot 1 = X$	
3.	$X + 1 = 1$	4.	$X \cdot 0 = 0$	
5.	$X + X = X$	6.	$X \cdot X = X$	
7.	$X + \bar{X} = 1$	8.	$X \cdot \bar{X} = 0$	
9.	$\overline{\bar{X}} = X$			
10.	$X + Y = Y + X$	11.	$XY = YX$	Commutative
12.	$X + (Y + Z) = (X + Y) + Z$	13.	$X(YZ) = (XY)Z$	Associative
14.	$X(Y + Z) = XY + XZ$	15.	$X + YZ = (X + Y)(X + Z)$	Distributive
16.	$\overline{X + Y} = \bar{X} \cdot \bar{Y}$	17.	$\overline{X \cdot Y} = \bar{X} + \bar{Y}$	DeMorgan's

□ **TABLE 2-7**

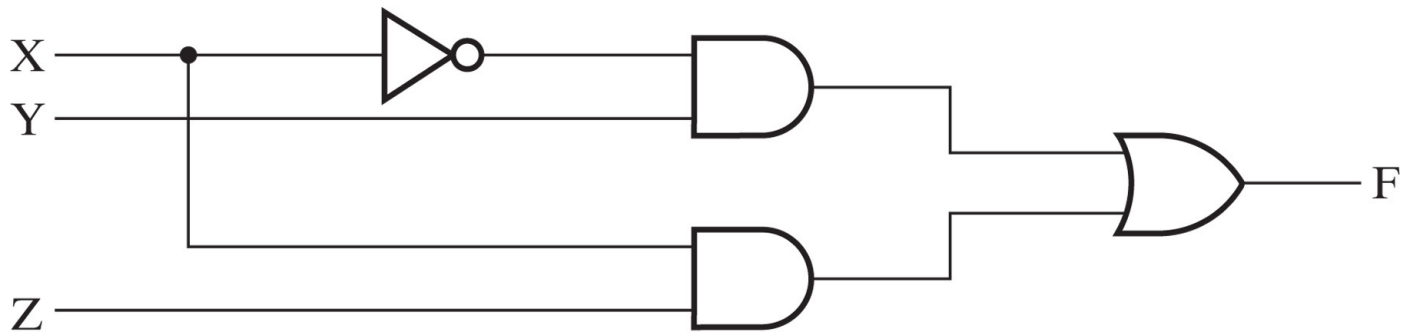
Truth Tables to Verify DeMorgan's Theorem

(a) X	Y	X + Y	$\overline{X + Y}$	(b) X	Y	\bar{X}	\bar{Y}	$\bar{X} \cdot \bar{Y}$
0	0	0	1	0	0	1	1	1
0	1	1	0	0	1	1	0	0
1	0	1	0	1	0	0	1	0
1	1	1	0	1	1	0	0	0

FIGURE 2-8 Implementation of Boolean Function with Gates



(a) $F = \bar{X}YZ + \bar{X}Y\bar{Z} + XZ$



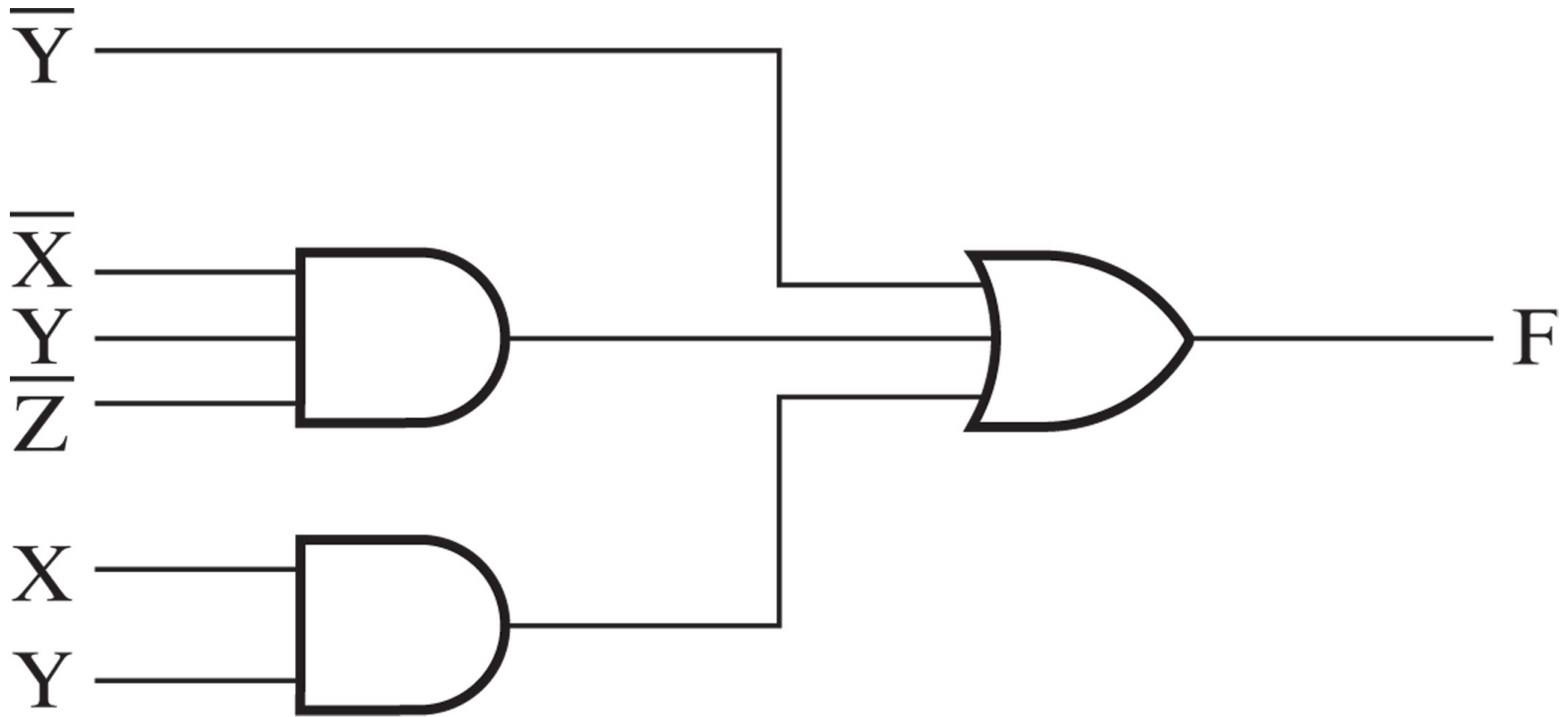
(b) $F = \bar{X}Y + XZ$

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□ TABLE 2-11
Boolean Functions of Three Variables

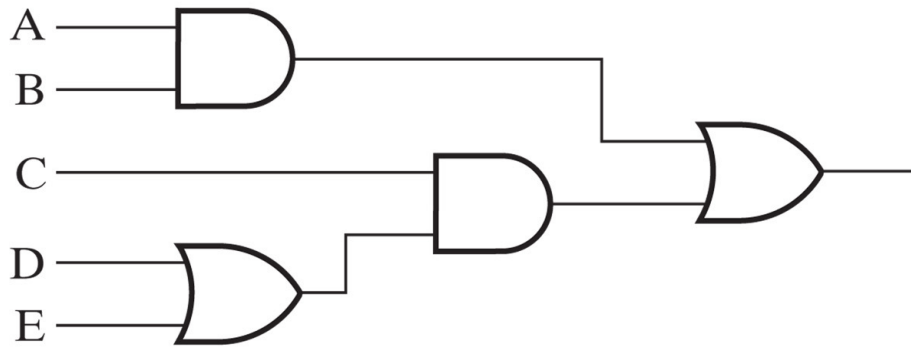
(a)	X	Y	Z	F	\bar{F}	(b)	X	Y	Z	E
	0	0	0	1	0		0	0	0	1
	0	0	1	0	1		0	0	1	1
	0	1	0	1	0		0	1	0	1
	0	1	1	0	1		0	1	1	0
	1	0	0	0	1		1	0	0	1
	1	0	1	1	0		1	0	1	1
	1	1	0	0	1		1	1	0	0
	1	1	1	1	0		1	1	1	0

FIGURE 2-9 Sum-of-Products Implementation

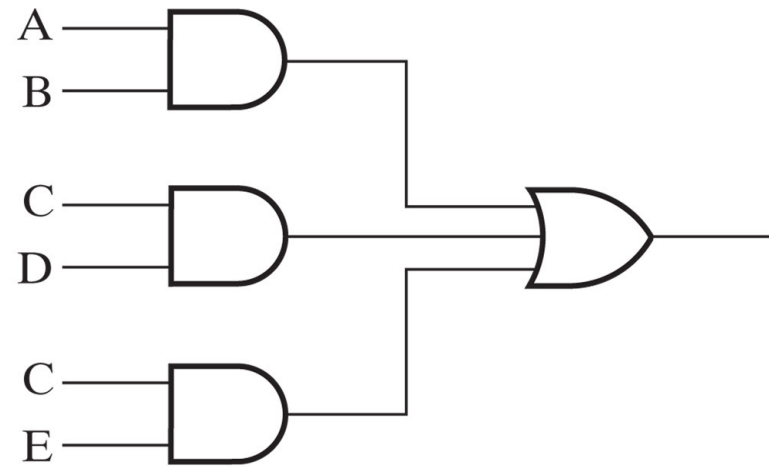


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FIGURE 2-10 Three-Level and Two-Level Implementation



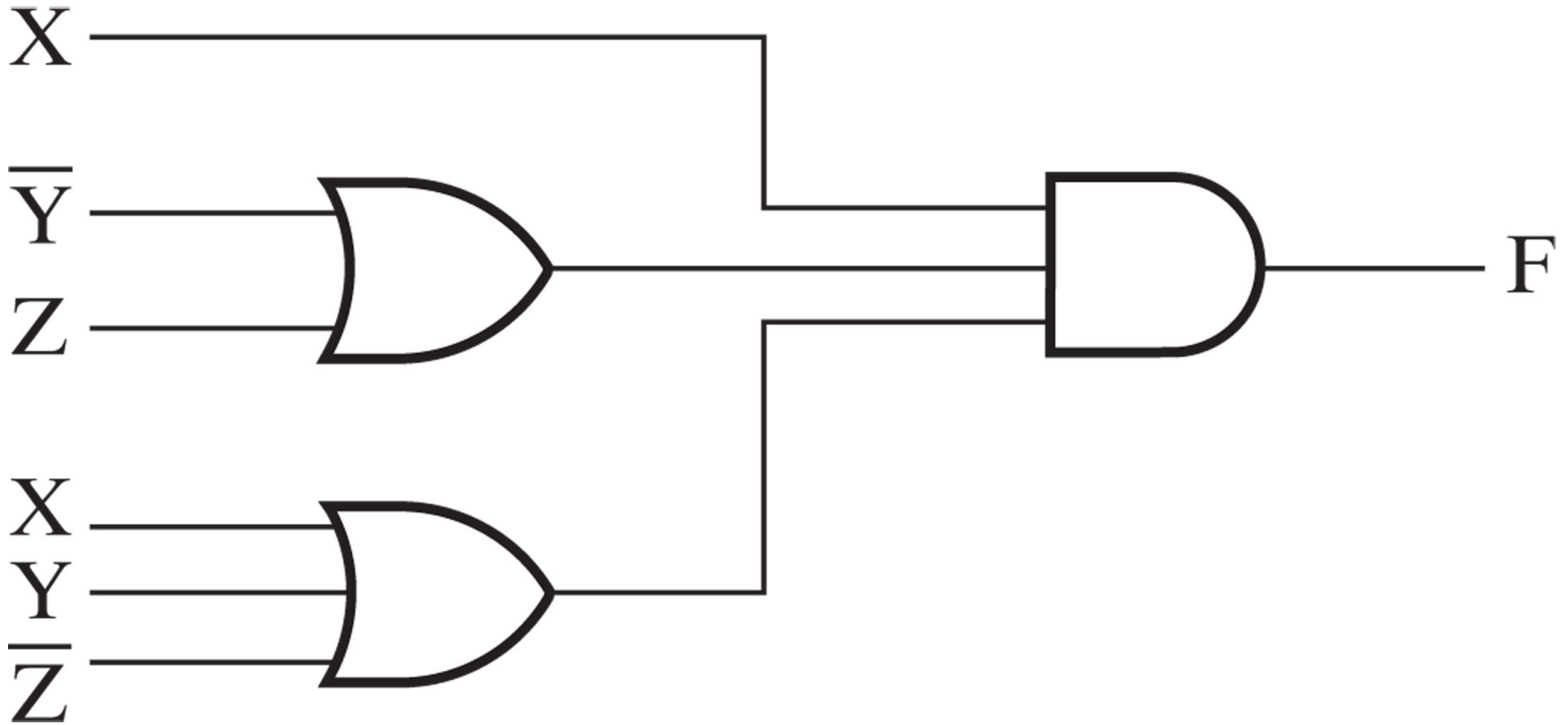
(a) $AB + C(D + E)$



(b) $AB + CD + CE$

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FIGURE 2-11 Product-of-Sums Implementation

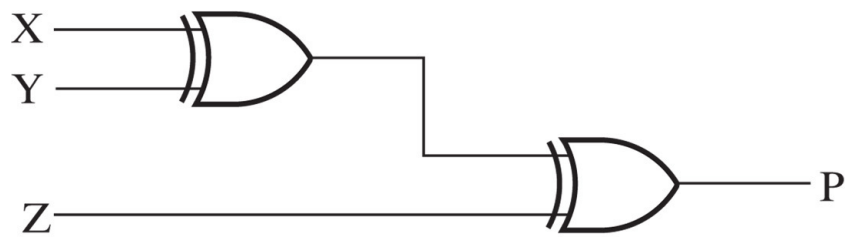


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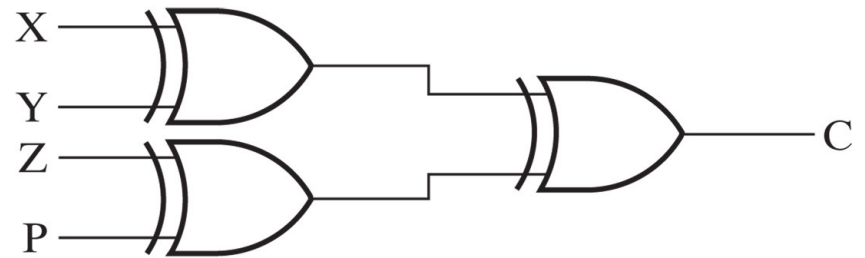
□ TABLE 2-12
Two-Variable Function F(A, B)

A	B	F
0	0	1
0	1	1
1	0	0
1	1	1

FIGURE 2-23 Multiple-Input Odd Functions



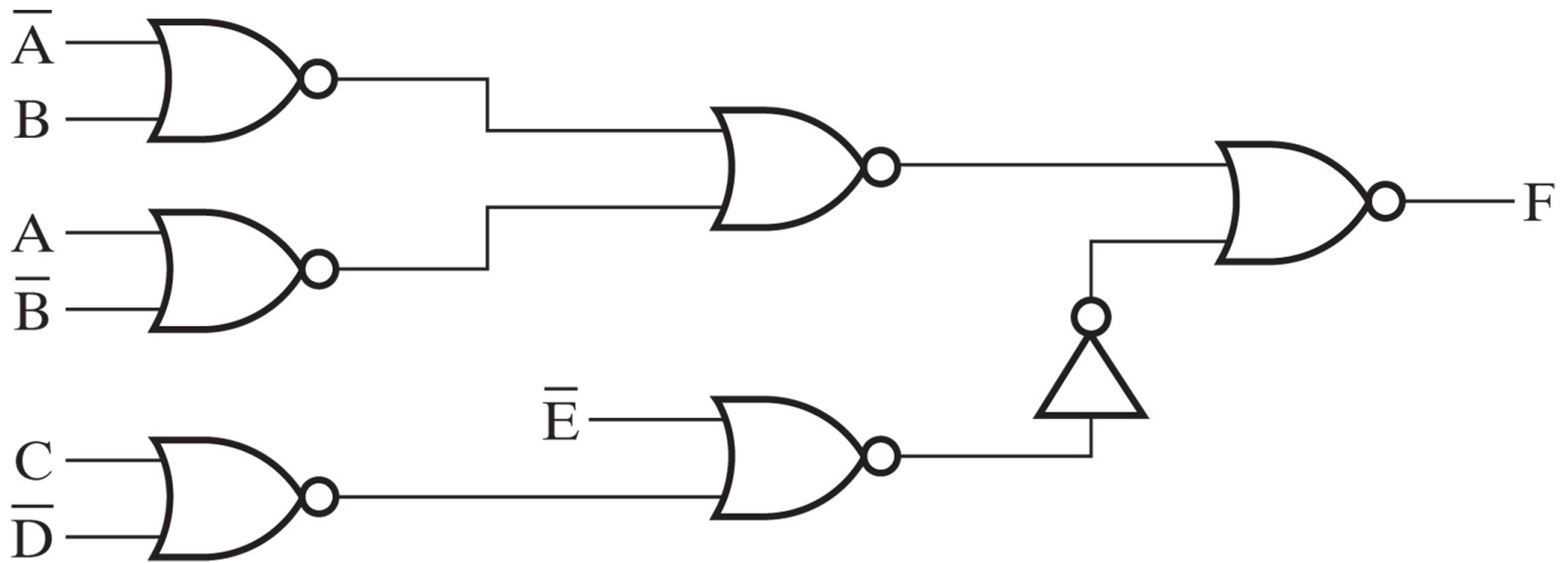
(a) $P = X \oplus Y \oplus Z$



(b) $C = X \oplus Y \oplus Z \oplus P$

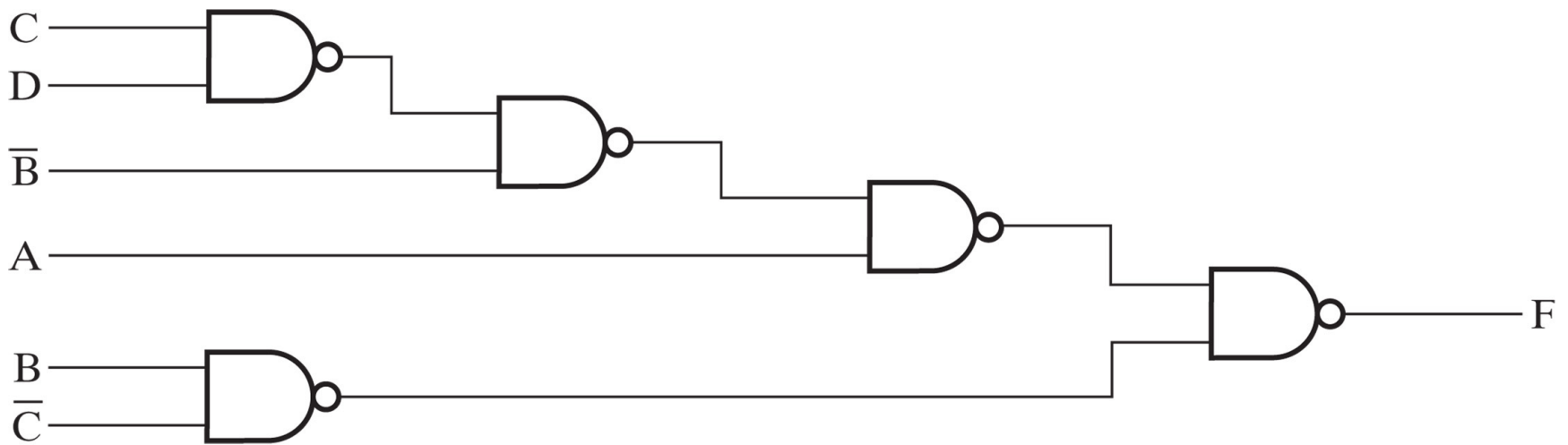
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FIGURE 2-39 Circuit for Problem 2-29



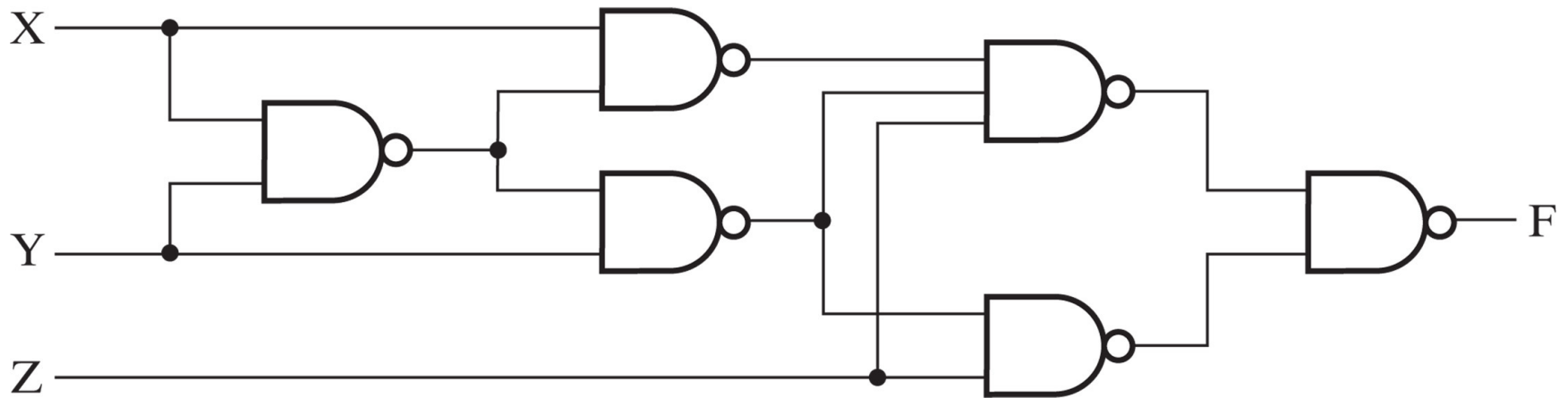
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FIGURE 2-41 Circuit for Problem 2-31



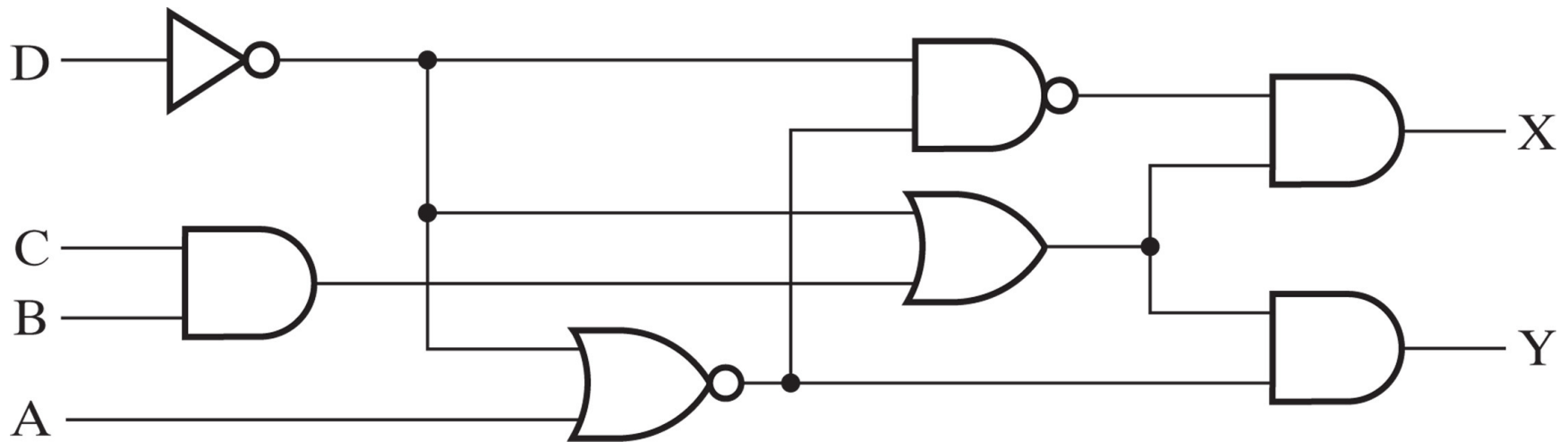
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FIGURE 2-43 Circuit for Problem 2-35, 2-38, 2-41, and 2-43



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FIGURE 2-44 Circuit for Problems 2-36 and 2-40



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